CLAIMS

What is claimed is:

1. A method of forming an integrated circuit package, the method comprising:

forming a lead frame having a plurality of conductors and at least one alignment feature electrically isolated from the plurality of conductors;

coupling at least some of the plurality of conductors to a semiconductor die; and

encapsulating the semiconductor die and a portion of the lead frame with an insulating material.

2. The method of claim 1, further comprising removing the at least one alignment feature.

3. A method of forming an integrated circuit package, the method comprising:

providing a plurality of conductors and at least one alignment feature;

coupling at least some of the plurality of conductors to a semiconductor die; and

encompassing the semiconductor die, the at least one alignment feature, and a portion of each of the plurality of conductors with an insulating material.

4. A method of forming and testing an integrated circuit package, the method comprising:

providing a plurality of conductors and at least one alignment feature;

coupling at least some of the plurality of conductors to a semiconductor die;

encompassing the semiconductor die, the at least one alignment feature, and a portion of each of the plurality of conductors with an insulating material;

coupling the at least one alignment feature encompassed by an insulating material with a portion of the testing device; and

testing the integrated circuit package through at least some of the electrically coupled conductors.

5. An integrated circuit comprising:

a semiconductor die;

a plurality of conductors, at least some of which are coupled to the semiconductor die; and

at least one alignment feature separate from the plurality of conductors.

6. The integrated circuit package of claim 5, wherein the at least one alignment feature includes at least one aperture.

7. The integrated circuit package of claim 5, wherein the at least one alignment feature is semi-circular shaped.

8. The integrated circuit package of claim 5, further comprising an insulating material encompassing the semiconductor die and a portion of each of the plurality of conductors, the insulating material comprising a first end and a second end, wherein the at least one alignment feature comprises an alignment feature disposed on both the first end and the second end of the insulating material.

9. The integrated circuit package of claim 5, wherein the at least one alignment feature comprises a protuberance.

10. An integrated circuit comprising:

a semiconductor die;

a plurality of conductors, at least some of which are coupled to the semiconductor die;

at least one alignment feature; and

insulating material encompassing the alignment feature.

11. The integrated circuit package of claim 10, wherein the at least one alignment feature is an alignment cut-out.

12. The integrated circuit package of claim 10, wherein the at least one alignment feature includes at least one aperture.

13. The integrated circuit package of claim 10, wherein the at least one alignment feature is semi-circular shaped.

14. The integrated circuit package of claim 10, wherein the at least one alignment feature comprises a tie bar.

15. The integrated circuit package of claim 10 further comprising a lead frame having a first end and a second end, wherein the at least one alignment feature comprises an alignment feature disposed on both the first end and the second end of the lead frame.

16. The integrated circuit package of claim 10, wherein the at least one alignment feature comprises a protuberance.

17. A lead frame strip ready for cutting, the lead frame strip comprising a plurality of integrated circuit packages, each integrated circuit package comprising:
a semiconductor die;
a plurality of conductors, at least some of which are coupled to the semiconductor die;
insulating material encompassing the semiconductor die and portions of the plurality of conductors; and
at least one alignment feature electrically isolated from the plurality of conductors.

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